CLAIM LISTING

1. (Currently AMended) A system for displaying images on a display, said system comprising:

a decoder for decoding encoded images and parameters associated with the images, thereby resulting in decoded images and ~~decoder~~ decoded parameters associated with the decoded images;

image buffers for storing the decoded images;

a ~~queue~~ FIFO for storing indicators indicating images to be displayed; and

a display engine for presenting the images indicated by the ~~queue~~ FIFO for display.


2. (Original) The system of claim 1, further comprising:

parameter buffers for storing the decoded parameters associated with the images.


3. (Original) The system of claim 2, wherein the display engine presents the images indicated by the queue for display by receiving the decoded parameters and displaying the decoded images based on the decoded parameters.


4. (Original) The system of claim 1, wherein the decoder comprises a first processor and the display engine comprises a second processor.

5. (Currently Amended) A method for displaying images on a display, said method comprising:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;

storing the decoded images;

queuing indicators indicating images to be displayed in a FIFO; and

presenting the images indicated by a particular one of the indicators for display.


6. (Original) The method of claim 5, further comprising:

storing the decoded parameters associated with the images.


7. (Original) The method of claim 6, wherein presenting the images for display further comprises receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

8. (Currently Amended) A circuit for displaying images on a display, said circuit comprising:

a processor;

a memory operably coupled to the processor, said memory storing a plurality of executable instructions, wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;

storing the decoded images;

~~queuing~~ storing indicators indicating images to be displayed in a FIFO; and

presenting the images indicated by the ~~queued~~ stored indicators for display.


9. (Original) The circuit of claim 8, further comprising:

storing the decoded parameters associated with the images.


10. (Original) The circuit of claim 9, wherein the instructions causing presenting the images further comprise instructions causing receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

11. (Currently Amended) A circuit for displaying images on a display, said circuit comprising:

a first processor;

a first memory operably coupled to the first processor, said first memory storing a plurality of instructions for execution by the first processor, wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;

storing the decoded images;

storing indicators indicating images to be displayed in a FIFO ~~queue~~; and

a second processor operably coupled to the queue;

a second memory operably coupled to the second processor, said second memory storing a plurality of instructions for execution by the second processor, wherein the plurality of executable instructions cause:

presenting the images indicated by the indicators for display.


12-15. (Cancelled)


16. (Previously Presented) The system of claim 1, wherein the queue stores the indicators in a particular order, and wherein the display engine displays the picture associated with the indicators in an order corresponding to the order that the indicators are stored in the queue.